WA 20.1: A DC Measurement IC with 130nV$_{pp}$ Noise in 10Hz

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A DC measurement IC consists of an instrumentation amplifier, a 4th-order ΣΔ modulator, a digital filter and a serial interface. The input amplifier uses chopper stabilization and multipath feedforward compensation to achieve 130nV$_{pp}$ in 10Hz and <70nV/°C offset drift in 0.6μm CMOS.

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Rough Charge Buffer

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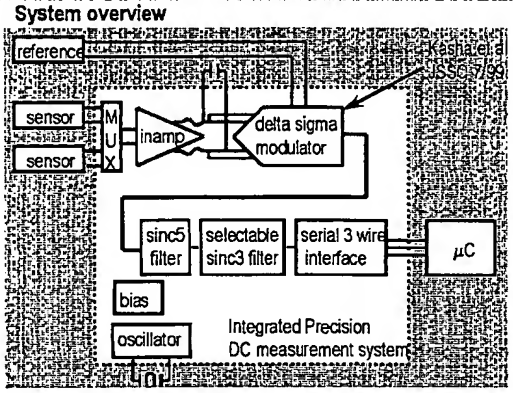
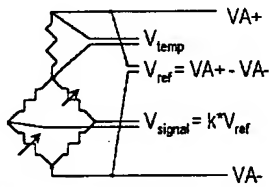
System overview

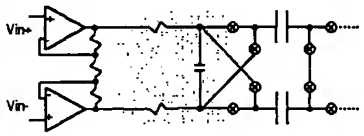


Introduction: application as bridge transducer IC

- 5mV full scale signal
- Low noise, low drift instrumentation amplifier required - an amplifier with the noise of a low noise bipolar and the DC stability of a chopper
- Large offset possible: high resolution ADC simplifies system

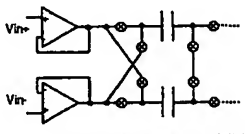


Implementation of amplifier/ADC interface



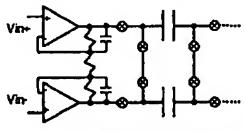
No noise aliasing: Amplifier wideband noise is removed
BUT:
Antialias filter records glitches and chop artifacts
Sampling does not happen from amplifier output
➡voltage drop across anti alias resistor can cause errors

Prior art: discrete time systems with higher noise



McCartney et al., JSSC 7/97

Excellent gain drift, but even with a noise free amplifier 6nV/rtHz would require more than 100pF switched at 4MHz



Kerth/Piasecki JSSC 12/92

Amp needs enough bandwidth to settle switched cap accurately at slow corner. Wide bandwidth leads to aliasing of noise.

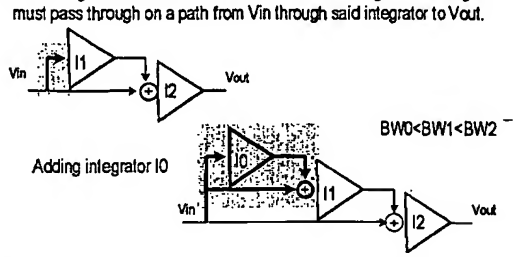
Amplifier design considerations

Use chopper stabilization to remove 1/f noise and offset.
Minimize secondary offset sources in amplifier
Use multipath feedforward architecture to

- implement filtering of chop artifacts
- avoid unnecessary power consumption in output stage
- avoid difficulty in stabilization caused by large input stage transconductance

Amplifier architecture development

- Any wire in or out of an integrator can be replaced with an integrator with bypass
- Each integrator must have lower UGBW than all integrators the signal must pass through on a path from Vin through said integrator to Vout.



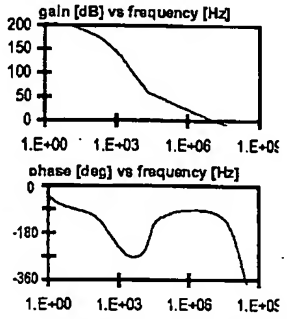
A closer look at the Bode plot

4 stages create 200dB of gain at DC and more than 100GHz GBW at 800Hz (simulated)

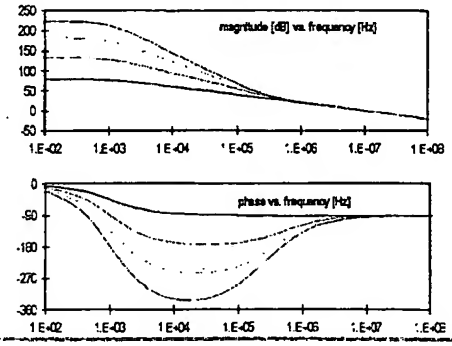
4th order transition allows -24dB/oct between band edge and UGBW

Phase lag can reach 360 degrees

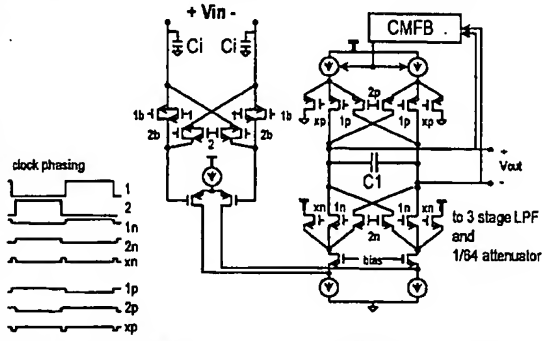
Multipath feedforward compensation: 3 LHP zeroes cause transition from 4th order slope to first order slope before UGBW



Opamp architecture: Bode plot

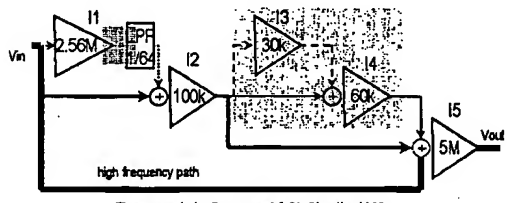


Implementation of chopper using current steering



Prior art: 5 stage amplifier

- I1 is chopper stabilized for <1μV offset
- 10mV of offset in I2 will appear as 640mV offset at the output of I1, 64μV of offset input referred



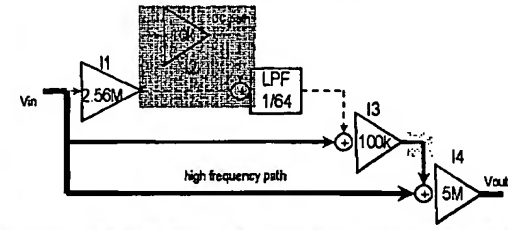
Thomsen et al., Symp. on VLSI Circuits, 1998

Chopper considerations

- filtering at input and output to avoid artifacts in amplified signal: 50pF on input, 3 pole LPF on output
- minimize glitches on output by using current steering instead of voltage switching
- current steering performed with low swing clocks
- signal during phase crossover not integrated on C1

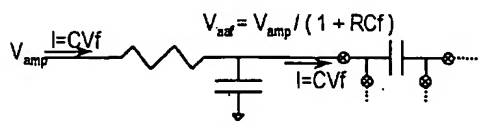
New architecture of the amplifier

- I1 is chopper stabilized for <1μV offset
- 10mV of offset of I3 appears as 640mV at the output of I2, 64nV at input of I1
- 10mV of offset of I2 appears as 1μV at the input of I1



Amp/ADC interface: need for rough charge buffer

- Dynamic current drawn by ADC causes voltage drop in anti-alias filter (AAF)
- No matching of AAF resistor to switched capacitor dynamic current => temperature coefficient of the gain.



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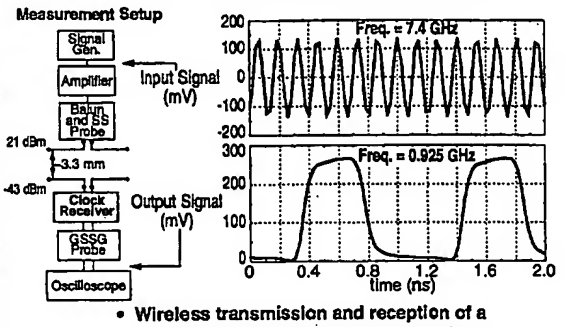
Antennas with Circuits: Antenna/Receiver



- **Wireless transmission and reception of a clock signal is demonstrated at ~8 GHz.**

Conclusions

- 0.25-µm clock receiver circuits have been implemented, including a 7.4-GHz LNA and a 10-GHz frequency divider.
- On-chip antennas have been implemented with CMOS receiver circuits.
- A transmitted 7.4-GHz global clock signal has been successfully received by a clock receiver over a ~4-mm distance (with interference structures), and a 925-MHz local clock signal is generated
- A single-receiver wireless interconnect for clock distribution has been demonstrated.
- Greatly improved performance is expected for 18-GHz operation, using a more advanced CMOS technology.

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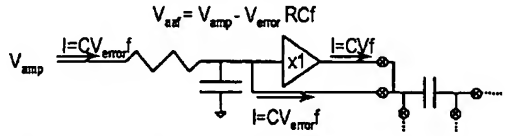
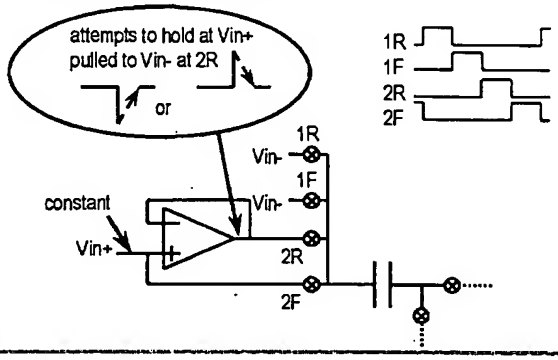
Amp/ADC interface: rough charge buffer requirement

- Rough charging required. Now input current is only V_{error}*f*C.
- Rough charging can have power requirements of the same order as integrator 1 amplifier
- Rail to rail input swing desired

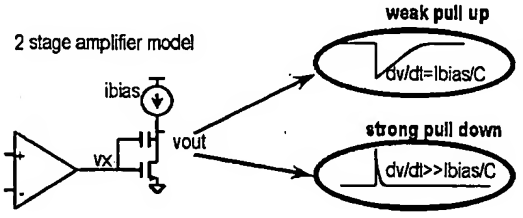


Rough charge buffer: Objective



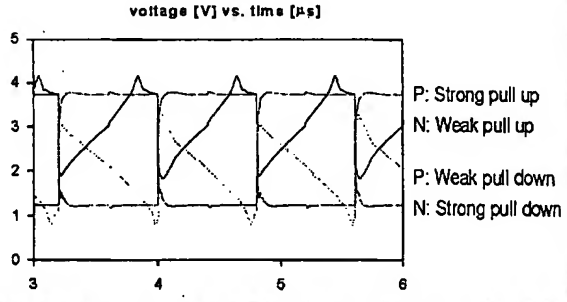
Rough charge buffer: idea

- Asymmetry: feedthrough through Miller cap allows strong pull-up/weak pull down (or vice versa)



at high frequency vx follows vout

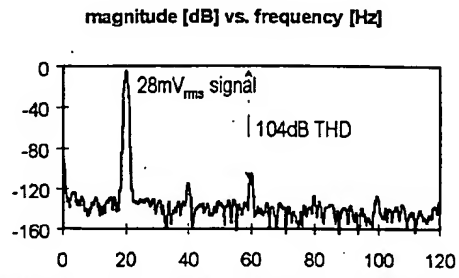
Simulation results of rough charge buffer



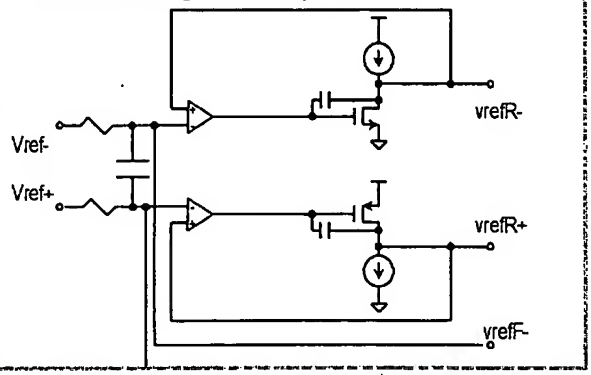
Rough charge buffer continued

- asymmetric response allows faster pull down without extra quiescent current
- much simpler than any class AB or slew boost scheme
- property of 2 stage amp can be easily exploited in reference input where vref+ > vref-
- signal input has bipolar input, wide common mode range
- to exploit property on signal input requires two output stages selectable by a comparator

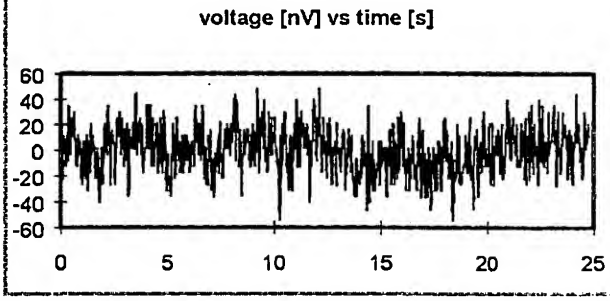
Experimental results: distortion (36dB gain)



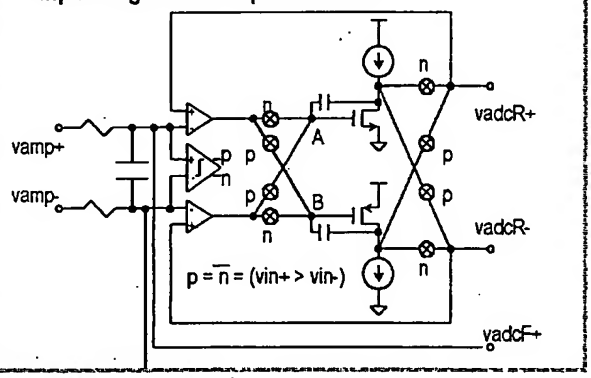
Reference rough buffer implementation



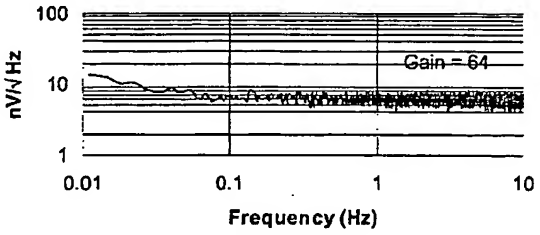
Experimental results: noise in 10Hz (36dB gain)



Input rough buffer implementation



Experimental results: noise spectrum



Observation of rough charging operation

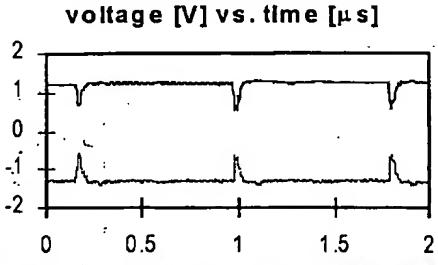


Table of noise and resolution results

inamp noise density 0.1 to 1000Hz	6.2nV / sqrt(Hz)
inamp peak to peak noise 0.1 to 10Hz	130nV
adc noise density 0.1 to 500Hz	70nV / sqrt(Hz)

Gain setting [dB]	full scale [mV$_{pp}$]	SNR in 2Hz [dB]	Noise free bits
36	80	129	20
30	160	135	21
6	2560	144	22.5

Output Word Rate 7.5Hz, 3dB frequency of digital filter 2Hz

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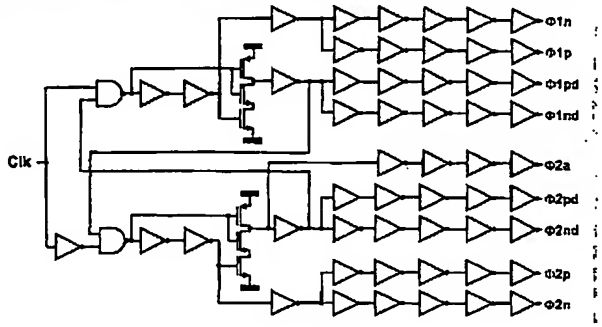
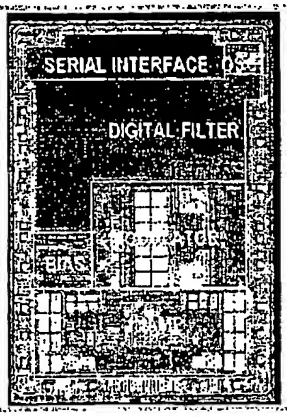
Table of measured results

technology	0.6µm double poly CMOS
die area	16 mm²
non-linearity/THD	0.0007%/-104dB
power consumption	50 mW from 5V
offset ADC only	1mV
offset amplifier	<1µV
offset drift ADC only (0dB gain)	700nV/°C
offset drift system (36dB gain)	15nV/°C
gain drift (36dB gain)	5ppm/°C
gain range	0 - 36 dB
output word rate	selectable 7.5Hz to 3840Hz

Clock Driver



Chip photo

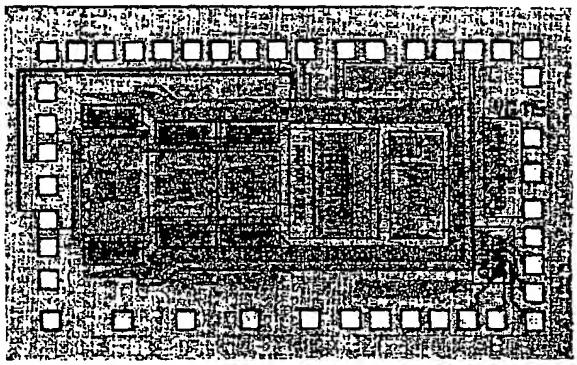


Layout Issues

- Fully symmetrical layout
- Avoid cross-talk: Vref's
- Dummies used to provide identical surroundings
- Several bondwires used to reduce inductance
- Large on-chip decoupling capacitance

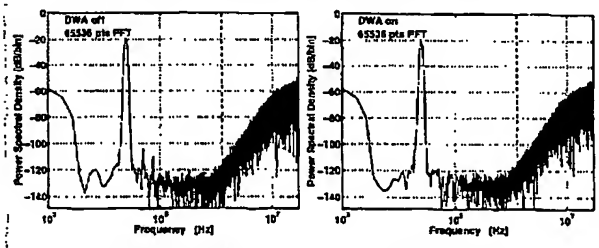
Conclusion

- Multipath feedforward compensated amplifier optimized for low offset, low noise, and low power
- 6nV/rtHz noise achieved using chopper stabilization, no aliasing
- Low power two stage rough charge buffer implementation
- Successful integration with 24 bit power managed delta sigma adc, digital filter and serial interface
- Lowest noise integrated DC measurement solution with 130nV$_{pp}$ in 0-10Hz without power penalty



Measurement results (1)

Effect of the DWA-algorithm



DWA off DWA on

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